UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte SEIJI ANDOH

Appeal No. 2006-1235
Application No. 09/376,063

ON BRIEF

Before THOMAS, KRASS, and JERRY SMITH, *Administrative Patent Judges.*
JERRY SMITH, *Administrative Patent Judge.*

DECISION ON APPEAL

This is a decision on the appeal under 35 U.S.C. § 134 from the examiner's rejection of claims 20, 22, 24-29, and 31, which constitute all the claims pending in this application.

The disclosed invention pertains to a package structure for a semiconductor device that has radiation solder bumps and connection solder bumps on the back surface of a substrate for surface mounting the semiconductor device to a printed circuit board. More particularly, the invention comprises two groups of solder bumps: (1) a first bump unit disposed in a central area of the back surface where the bumps are disposed a first distance apart from each other, and (2) a second bump unit formed in the peripheral area of the back surface where the bumps are disposed a second distance apart that is greater than the first distance. An intermediate area without bumps is located between the central area and peripheral area and separates the two bump units. The width of the intermediate area is greater than the spacing between the bumps in the second bump unit.

The first bump unit carries no electrical signals, but rather radiates heat from the semiconductor device to the surface to which it is mounted. The second bump unit, however, transmits signals to and from the semiconductor device to the printed

circuit board to which it is mounted. By spacing the solder bumps in the first bump unit closer together than the bumps in the second bump unit, upon heating, bumps in the first bump unit will fuse together as a unitary body to enhance heat transfer from the semiconductor device. The bumps in the second bump unit, however, will remain apart from each other thus avoiding short circuits caused by solder bridges.

Representative claim 20 is reproduced as follows:

20. A semiconductor device, comprising:

a substrate having a main surface and a back surface, wherein said back surface has a central area, a distinct intermediate area in which no bumps are disposed, surrounding said central area, and a peripheral area surrounding said intermediate area;

a semiconductor chip disposed on said main surface;

a first bump unit disposed in said central area of said back surface, wherein said first bump unit includes a plurality of bumps that are disposed a first distance apart from each other, and wherein said first bump unit radiates heat from said semiconductor device; and

a second bump unit formed in said peripheral area of said back surface, wherein said second bump unit includes a plurality of bumps that are disposed a second distance apart from each other, said second distance is greater than said first distance, and said second distance is less than a third distance between said central area and said peripheral area, and

wherein said second bump unit transmits signals.

The examiner relies on the following reference:

Bond et al. (Bond) 5,642,261 Jun. 24, 1997

The following rejection is on appeal before us:

Claims 20, 22, 24-29, and 31 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Bond.

Rather than repeat the arguments of appellant or the examiner, we make reference to the brief and the answer for the respective details thereof.

OPINION

We have carefully considered the subject matter on appeal, the rejection advanced by the examiner and the evidence of obviousness relied upon by the examiner as support for the rejection. We have, likewise, reviewed and taken into

consideration, in reaching our decision, the appellant's arguments set forth in the brief along with the examiner's rationale in support of the rejection and arguments in rebuttal set forth in the examiner's answer.

It is our view, after consideration of the record before us, that the evidence relied upon and the level of skill in the particular art would not have suggested to one of ordinary skill in the art the obviousness of the invention as set forth in the claims on appeal. Accordingly, we reverse.

In rejecting claims under 35 U.S.C. § 103, it is incumbent upon the examiner to establish a factual basis to support the legal conclusion of obviousness. See In re Fine, 837 F.2d 1071, 1073, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). In so doing, the examiner is expected to make the factual determinations set forth in Graham v. John Deere Co., 383 U.S. 1, 17, 148 USPQ 459, 467 (1966), and to provide a reason why one having ordinary skill in the pertinent art would have been led to modify the prior art or to combine prior art references to arrive at the claimed invention. Such reason must stem from some teaching, suggestion

or implication in the prior art as a whole or knowledge generally available to one having ordinary skill in the art. Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 1051, 5 USPQ2d 1434, 1438 (Fed. Cir.), cert. denied, 488 U.S. 825 (1988); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 293, 227 USPQ 657, 664 (Fed. Cir. 1985), cert. denied, 475 U.S. 1017 (1986); ACS Hosp. Sys., Inc. v. Montefiore Hosp., 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984). These showings by the examiner are an essential part of complying with the burden of presenting a prima facie case of obviousness. See In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). If that burden is met, the burden then shifts to the applicant to overcome the prima facie case with argument and/or evidence. Obviousness is then determined on the basis of the evidence as a whole and the relative persuasiveness of the arguments. See id.; In re Hedges, 783 F.2d 1038, 1039, 228 USPQ 685, 686 (Fed. Cir. 1986); In re Piasecki, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984); and In re Rinehart, 531 F.2d 1048, 1052, 189 USPQ 143, 147 (CCPA 1976). Only those arguments

actually made by appellant have been considered in this decision. Arguments which appellant could have made but chose not to make in the brief have not been considered and are deemed to be waived [see 37 CFR § 41.37(c)(1)(vii)(2004)].

The examiner argues that Bond teaches a semiconductor device including two distinct groups of solder bumps that constitute the first and second bump units respectively [answer, page 6]. The examiner notes that the first bump unit of Bond is formed in the heat-radiating central area of the substrate 14, and the second bump unit is formed in the "signal peripheral area" [id.].

The examiner contends that the bumps comprising the first bump unit are disposed sufficiently close together so that the bumps are "inherently capable" of melting together upon applying heat [answer, page 7]. To support this contention, the examiner primarily relies on Fig. 2 of Bond that, according to the examiner, shows the solder bumps 18 touching each other [answer, pages 7 and 9]. The examiner further asserts that the bumps comprising the second bump unit will inherently remain apart from each other upon applying heat [answer, page 7].

The examiner admits that Bond does not disclose that the second distance (i.e., distance between the bumps in the second bump unit) is less than the width of the intermediate area between the first and second bump units. The examiner, however, contends that manipulating sizes of solder balls and distances between them is well known in the art to avoid shorting during reflow processes [answer, pages 8 and 11]. Also, the examiner asserts that such a modification involves a mere change in component size or range of distances between them, and that it has been held that where the general conditions of a claim are disclosed in the prior art, discovering optimum or workable ranges involves only routine skill in the art [answer, page 8]. The examiner concludes that it would have been obvious to one of ordinary skill in the art at the time of the invention to arrange the solder bumps of Bond with the claimed relative distances to avoid shorting the bumps in the signal peripheral area and to increase heat dissipation [answer, page 8].

Appellant argues that although Bond generally discloses central and peripheral areas of solder bumps with thermal and signal transfer functions respectively, Bond does not disclose any requirement regarding the respective spacings within or between the bump units [brief, pages 12 and 13]. Appellant argues that Bond appears to show that the spacing between bumps is "generally the same" [brief, page 12]. Appellant further argues that the examiner's sole reliance on Fig. 2 of Bond is unwarranted since Fig. 1 is a cross-sectional figure taken along section line "1-1" of Fig. 2 that "reveals far more detail than Figure 2" [brief, page 16]. Appellant notes that Fig. 1 shows that the solder balls 18 under conductive slab 12 do not contact each other and do not appear to be any closer to each other than the solder balls in the peripheral area [id.].

Appellant further contends that Bond lacks a distinct intermediate area devoid of solder bumps that has a width greater than the distance between bumps in the peripheral area. According to appellant, Bond discloses no clear gap between the central and peripheral areas.

We will not sustain the examiner's obviousness rejection. As best seen in Fig. 1, Bond discloses (1) a first bump unit comprising a central array of solder balls directly below conductive slug 12 for radiating heat from the semiconductor device, and (2) a second bump unit comprising a separate peripheral array of solder balls directly below vias 19 for transmitting signals. Contrary to appellant's assertion, Bond in Fig. 1 shows an unlabeled intermediate area devoid of bumps that surrounds the central array of bumps directly below conductive slug 12 (i.e., the gap between the outermost solder balls below conductive slug 12 and the innermost solder balls connected to vias 19).

Bond, however, does not reasonably teach nor suggest the relative spacing between the bumps in the first and second bump units respectively in conjunction with the relative spacing between the bump units established by the intermediate area as

claimed in the independent claims. As appellant notes, Fig. 1 of Bond is a cross-sectional view taken along section line 1-1 in Fig. 2. Although Fig. 2 shows solder bumps 18 in dashed lines that are closely adjacent to each other in the central region, the more detailed cross-sectional view, Fig. 1, reveals discrete gaps between the bumps in the central region.

Nevertheless, it is well settled that patent drawings are generally not drawn to scale and may not be relied upon to define the precise proportions of the elements or show particular sizes if the specification is completely silent on the issue. Hockerson-Halberstadt, Inc. v. Avia Group Int'l, 222 F.3d 951, 956, 55 USPQ2d 1487, 1491 (Fed. Cir. 2000). With this fundamental principle in mind, we cannot conclusively determine the actual and relative distances between the solder bumps solely by inspecting the figures of Bond. Rather, we must turn to the specification of Bond for guidance.

Bond, however, does not provide further details regarding the relative spacing of the solder bumps shown in Figs. 1 and 2. For example, in col. 4, lines 34-38, Bond notes that the solder balls 18 are "disposed in an array manner beneath and in contact with slug 12[,] for providing thermal connection between slug 12 and a thermal conductor in system circuit board 20." Bond further notes that the solder balls are formed on the underside of substrate 14 and slug 12 "in the conventional manner, for example by way of a solder mask (not shown) on the underside of substrate 14" [Bond, col. 4, lines 62-65]. See also Bond, col. 4, lines 15-20 (noting that the solder balls are arranged "in the conventional ball-grid-array manner" and correspond to lands or other surface conductors on the top surface of the circuit board). These general statements do not provide a sufficient teaching or suggestion to the skilled artisan to dispose the solder balls in the central and peripheral regions with the relative spacings claimed, let alone with a spacing distance that is relative to the intermediate area distance as claimed in the independent claims.

On this record, we cannot agree with the examiner that the solder bumps of the first bump unit (i.e., directly below the conductive slug 12) touch each other and are inherently capable of melting together due to their relative proximity shown in Fig. 2. Such assertions are mere conclusory statements that are, at best, speculative given the record before us.

Core factual findings in patentability determinations must point to some concrete evidence in the record to support the findings. In re Zurko, 258 F.3d 1379, 1386, 59 USPQ2d 1693, 1697 (Fed. Cir. 2001). In addition, obviousness rejections must be based on evidence comprehended by 35 U.S.C. § 103. In re Lee, 277 F.3d 1338, 1342, 61 USPQ2d 1430, 1433 (Fed. Cir. 2002) (emphasis added). See also In re Kahn, 78 USPQ2d 1329, 1336 (Fed. Cir. 2006) ("[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.").

We note the examiner's rationale regarding installing a separate packaged integrated circuit to a system circuit board on pages 9 and 10 of the answer, but such an installation hardly guarantees that the solder bumps of the first bump unit would fuse together. Rather, it is equally plausible that, upon heating, the solder bumps would maintain gaps between them, yet bond the component to the underlying board and transfer heat. See, e.g., Fig. 6 of Bond (disclosing spaced leads 80' formed after reflowing solder balls). There is simply no evidence in the record before us that supports the examiner's conclusion that the solder bumps would fuse together upon heating.

Furthermore, on this record, we cannot agree that it would have been obvious to the skilled artisan to modify solder ball sizes and distances between them to achieve the results stated by the examiner absent some teaching or suggestion to do so. We disagree with the examiner that the claimed relative spacing between solder bumps amounts to discovering the optimum or

workable ranges involving only routine skill in the art where the general conditions of the claim are disclosed in the prior art. The claimed relative spacings and distances are more than mere optimizations of result-effective variables. Rather, the claimed relative distances are critical to achieve the invention's objective -- namely to prevent short circuits caused by solder bridges between the bumps of the second bump unit, yet improve thermal conductivity between the semiconductor device and its mounting surface via the closer proximity of the bumps in the first bump unit. Apart from the examiner's conclusory statements, nothing in the record before us teaches or suggests adjusting the relative spacing in the manner claimed.

We note, however, that the respective functions of the central and peripheral bump units of Bond are identical to those of the claimed invention -- namely heat transfer and signal transmission respectively. If the examiner had appropriately combined Bond with an analogous secondary prior art reference expressly teaching arranging solder balls or bumps so close

together or touching each other so that they would fuse together upon applying heat to improve heat transfer, we may have reached a different conclusion. Absent an express teaching from the prior art to support the examiner's conclusion regarding the claimed relative spacings, however, we must resort to speculation. That we will not do.

In summary, we have not sustained the examiner's rejection with respect to any of the claims on appeal. Therefore, the decision of the examiner rejecting claims 20, 22, 24-29, and 31 is reversed.

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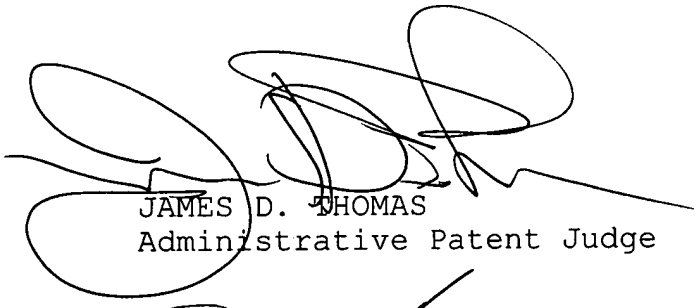
REVERSED



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